**Jonathan Reyes**

6320 17TH Ave N · St Petersburg, FL 33710

Phone: 786-547-4835 · Email: jmr533@gmail.com

**Work Experience**

**IBM | Austin, TX**

*Advisory Physical Design Engineer Lead – zSystems* August 2015 - Present

* z17 DD1 (5 nm)
  + Ring and MBus Units Circuit Lead
    - Represent Z Physical Design in an internal panel on the Telum processor
  + PD DevOps focal point
    - Educate/Train and Support the team as an expert user of Git and the new build system for PD tools
* z16 DD1/DD2 (7 nm)
  + Ring and MBus Units Circuit Lead
    - Lead a team of full-time engineers through all phases of the project including tapeout; provide continuous training and guidance to new hires and contractors in the construction flow and signoff checks
    - Interface with integration and logic design teams for bus planning and timing closure
  + Perform cross section analysis/implementation on critical chip paths
  + Trained zAustin team on new Git/DevOps AOD flow to improve design efficiency

*Staff Physical Design Engineer – zSystems*

* z14 DD1/DD2 + z15 DD1 (14 nm)
  + L4 Cache Circuit Designer
    - Performed cross section analysis and floorplanning through the initial phase of the project
    - Drove logic synthesis tools and pre-placement of IP
    - Place, route, and congestion analysis
    - Led area and power reduction effort for the largest blocks
    - Signoff checks including physical verification (LVS/DRC/Methodology checks), noise, electromigration, and RC extraction
    - Timing Closure and ECO during final design phase

Physical Design Engineer *– zSystems*

* z13 DD2 (22 nm)
  + Joined team in the last few months to help with Timing Closure, DRC/LVS cleanup, DTCAP Analysis, ECO

**IBM | Rochester, MN**

Physical Design Engineer *– POWER Systems* December 2012 - August 2015

* P8’ (22 nm)
  + Circuit (LBS) Designer with Embedded IP for N-Vidia Link Processing unit

*Physical Design Engineer/Intern – ASIC*

* FlankerCR (32 nm)
  + Owned fln\_amax RLM for entirety of the project and helped RIT closure of other RLMs
* SPA (65 nm)
  + Floor planning, Clock Tree Synthesis, Placement, Routing, Timing Closure, and Signoff using Cadence Encounter

**Education**

* Florida International University, Miami, FL GD: Fall 2011  
  Bachelor’s of Science in Computer Engineering